

## **REMARKS**

A final Office Action was mailed on August 25, 2004. Claims 1 – 13 are pending in the present application. With this Response, Applicants proposed revisions to FIGs. 1 and 12, amend the specification, cancel claims 10 and 13 without prejudice or disclaimer, and amend claims 1 – 9, 11 and 12. No new matter is introduced. Support for the claim amendments may be found, for example, in FIG. 3 and at page 11, line 30 to page 12, line 12 of Applicants' specification.

### **OBJECTION TO DRAWING**

The drawing is objected to under 37 C.F.R. § 1.83(a) because FIG. 1 fails to show “a switching apparatus 1” as described in the specification. Applicants propose an associated revision to FIG.1 to address this objection, and a revision to FIG. 12 to correct a minor error. These revisions are indicated in the attached drawing replacement sheets, provided in both marked-up and clean copies. Applicants respectfully request that the proposed revisions be accepted, and that the objection be withdrawn.

### **OBJECTION TO SPECIFICATION**

The specification is objected to in regard to informalities at page 11, lines 12 and 13. Applicants amend the specification to address these informalities, and respectfully request that the objection be withdrawn.

### **REJECTION UNDER 35 U.S.C. § 112**

Claims 1 – 13 are rejected under the second paragraph of 35 U.S.C. § 112 as being incomplete for omitting “essential structural cooperative relationships of elements”. Specifically,

the Examiner notes that while the preamble to independent claims 1, 4, 7, 10, 11 and 12 recites “a buffer unit for fragmenting variable-length packets into fixed-length packets for processing in units of fixed-length packets”, these claims and associated FIGs. 2, 7 and 10 fail to show means by which variable-length packets are transformed to fixed-length packets (i.e., each of the claims and FIGs. operate with respect to fixed-length packets only). Applicants amend the preambles of independent claims 1, 4, 7, 11 and 12 to recite “a buffer unit (switching apparatus) for processing fixed-length packets that have been fragmented from variable-length packets, said processing being performed in units of fixed-length packets”. Applicants thereby clarify that the claimed invention is concerned with the processing of fixed-length packets, for example, by monitoring a storage state of a fixed-length packet storing part, and carrying out a control so that multicasting packets are transferred between variable-length unicast packets formed from the fixed-length packets rather than being interleaved with fixed-length unicast packets forming the variable-length unicast packets (see, FIG. 3 and page 11, line 30 to page 12, line 12 of Applicants’ specification). Applicants therefore respectfully request that the rejection be withdrawn.

#### REJECTION UNDER 35 U.S.C. § 103

Claims 1, 2, 7, 8 and 11 - 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,825,767 to Mizukoshi et al. in view of U.S. Patent No. 6,714,562 to Calvignac et al. Claims 4, 5 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizukoshi in view Calvignac and U.S. Patent No. 5,898,687 to Harriman. Applicants cancel claims 10 and 13 without prejudice or disclaimer, amends claims 1 – 9, 11 and 12 to clarify the nature of their invention, and respectfully traverse these rejections.

In independent claims 1, 4, 7, 11 and 12, Applicants disclose a buffer unit for a switching apparatus that is arranged to process fixed-length packets that have been fragmented from

variable-length packets in units of fixed-length packets. The fixed-length packet fragments include unicasting packets and multicasting packets. As disclosed by each of independent claims 1, 4, 7, 11 and 12, outputs of the buffer unit are read in units of a variable-length packet which is formed by a plurality of fixed-length packets. As a result, interleaving of multicasting packets with the fixed-length unicast packets is prevented. For example, as disclosed by independent claim 1, Applicants claim:

1. A buffer unit for processing fixed-length packets ~~for~~ that have been fragmented from variable-length packets, said processing being performed in units of fixed-length packets, comprising:

a fixed-length packet storing configured to store the fixed-length packets for each of a plurality of output paths;

a multicasting processing part configured to store multicasting packets having a plurality of destinations, and to transfer the multicasting packets to said fixed-length packet storing part depending on the plurality of destinations; and

a control part configured to monitor a storage state of said fixed-length packet storing part, and to carry out a control so that the multicasting packets are transferred between a variable-length packet formed by a plurality of fixed-length packets and a next variable-length packet.

Mizukoshi discloses an ATM switch including a shared buffer and control means for controlling cell outputs from the buffer (see, e.g., abstract of Mizukoshi). The ATM switch of Mizukoshi includes means for storing multicast cells in the buffer and transferring mulitcast cells as cell outputs from the buffer (see, e.g., Figure 2 of Mizukoshi) The Examiner acknowledges that Mizukoshi fails to disclose fragmenting variable-length packets into fixed-length packets, and providing control means for sending multicast packets as variable-length packets formed by a plurality of fixed-length packets. The Examiner suggests that these limitations are however disclosed by Calvignac.

Calvignac discloses an apparatus for segmenting variable-length frames into fixed-length frames, and reassembling the fixed-length frames into variable-length frames (see, e.g., abstract

of Calvignac). Applicants respectfully submit that Calvignac however fails to disclose Applicants' claimed control part for monitoring a storage state of a fixed-length packet storing part and for controlling the transfer of multicasting packets to the fixed-length packet storing part so that "multicasting packets are transferred between a variable-length packet formed by a plurality of fixed-length packets and a next variable-length packet".

Harriman discloses a multicast logic engine that stores a single copy of a multicast data element in shared memory for which only an address pointer is replicated in order to provide multicasting capability (see, e.g., abstract of Harriman). Like Mizukoshi and Calvignac, Harriman fails to disclose or suggest Applicants' claimed buffer unit for controlling the defragmenting of fixed-length packets so that multicasting packets are transferred between a variable-length packet formed by a plurality of fixed-length packets and a next variable-length packet.

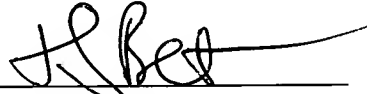
In summary, Applicants respectfully submit that independent claims 1, 4, 7, 11 and 12 are not made obvious by any combination of the cited references, and are therefore allowable. As claims 2, 3, 5, 6, 8 and 9 each depend from allowable claims 1, 4 and 7, Applicants respectfully submit that claims 2, 3, 5, 6, 8 and 9 are allowable for at least this reason.

## CONCLUSION

An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that 1 – 9, 11 and 12, which include independent claims 1, 4, 7, 11 and 12, and the claims that depend therefrom, stand in condition for allowance. Passage of this case to allowance is earnestly solicited. However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is

respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'TJ Bean', written over a horizontal line.

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